2021
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES
VIRTUAL | MARCH 1-4, 2021

DVCON UNITED STATES 2021 CONFERENCE PROGRAM

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DVCon U.S. 2021

Welcome Message from DVCon U.S. General Chair, Aparna Dey

General Chair – Aparna Dey, Cadence Design Systems, Inc.

I am pleased to welcome you to our virtual DVCon U.S. 2021 conference and exhibition! This year, DVCon will offer attendees a combination of recorded presentations and live Q&A to provide an interactive, high-quality virtual experience. Attendees can look forward to outstanding technical sessions and virtual discussions on many hot topics as well as networking during the virtual breakout sessions and opportunities to preview the latest industry design and verification tools and services from the best in the industry.

We are proud of continuing our tradition of providing an annual technical forum that serves the needs of the practicing design and verification community, organized by dedicated volunteers from the community itself.

Now in its 33rd year, DVCon U.S. has established itself as the must-attend industry and user-focused conference for practicing design and verification engineers, EDA developers, IP integrators and design managers, focusing on design and verification of electronic systems and integrated circuits. We are proud that this conference attracts wide participation from the industry from the smaller to the larger companies throughout the program and exhibition.

Our 4-day virtual program includes many key design and verification topics including RISC-V, cloud-based design, open source, formal verification, portable stimulus, IP security, UVM, functional safety, prototyping and emulation, SystemC, among others. The event provides an opportunity to discuss challenges and solutions that can be beneficial in current and upcoming projects as electronic designs and verification complexities and challenges continue to increase exponentially. Attendees will find each of these areas addressed at the conference's sessions, panels, posters, tutorials, and Workshops with an emphasis on solutions to engineers' real-world problems.

We are pleased to offer an in-depth technical program this year. We received over 160 outstanding submissions for papers, panels, tutorials, and Workshops from the best technical minds and organizations in the industry. Our focus on the users of Accellera standard EDA languages, tools, and methodologies continues to be a DVCon 2021 hallmark. Attendees can expect to learn about both practical solutions to their pressing problems and preview the technologies that will affect them in the near future.

One of the benefits of a virtual conference is the on-demand availability of the sessions. With such an extensive program, full-conference attendees will have access to the entire program and will not have to choose between parallel sessions. They can enjoy the recorded sessions at their leisure.

I am pleased to present the work of the DVCon Steering Committee and Technical Program Committee, who have put together an excellent 2021 program with the support of our conference management specialists, Conference Catalysts.

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Highlights of the conference include:

Accellera Day: On Monday, March 1, our conference sponsor, Accellera Systems Initiative, kicks off DVCon U.S. with Accellera Day. We will have a morning Accellera tutorial on Portable Stimulus focused on the standard's upcoming 2.0 version, as well as five Accellera Workshops presented by Accellera standards working group members. There will also be an Accellera-sponsored Birds of a Feather on UVM that will be part of the free registration option. We will have six sponsored Workshops in the afternoon presented by design verification industry members covering topics such as functional safety, HLS, ISO26262, functional SoC, harmonizing hardware and software, and verification management.

Keynote: This year's keynote, "Computational Logistics for System and Software Verification," will be given by Dr. Paul Cunningham, corporate vice president and general manager of the system verification group at Cadence. In his presentation Dr. Cunningham will introduce the concept of verification throughput and highlight the significant opportunities we have as an industry to dramatically improve verification throughput on modern SoC designs.

Technical papers and posters: Technical Program Chair, Vanessa Cooper, and Poster Chair, John Dickol, have organized an excellent technical program on Tuesday and Wednesday with 18 sessions that include 42 papers and 14 posters. We are very grateful for the outstanding submissions and the work done by the technical program committee volunteers to review the submissions and encourage the community to keep submitting. There are so many good choices that you will want to go through the program and review it thoroughly as you plan each day. There is something for everyone in this broad, in-depth technical program. With so many interesting options, we look forward to your votes for the best paper and best poster awards after the last program session on Wednesday.

Tutorials and Workshops: Ambar Sarkar, tutorial and Workshop chair, has put together an outstanding selection of tutorials and Workshops for Monday and Thursday. The Workshops are extremely popular and are intended to give more organizations, mostly smaller companies, greater opportunity to participate in the program and give attendees more variety in shorter educational and learning sessions. We have 13 sponsored Workshops in this year's program—seven on Monday and six on Thursday—covering a wide variety of topics.

We will have three sponsored tutorials on Thursday with topics covering: The Benefits of a Common Methodology for Emulation and Prototyping, Applying Big Data to Next-Generation Coverage Analysis and Closure, and Raising the Verification Bar: Cloud based Simulation Increases Verification Efficiency.

Panels: Tom Fitzpatrick, panel chair has organized two excellent panel sessions: "Verification in the Open-Source Era," and "Chip Design on Cloud - from Pipe Dream to Preeminence." Both panels will offer attendees an opportunity to ask questions during a live Q&A on the conference platform.

Virtual Exhibition: We are in the process of creating an interactive expo that will be a fun gathering place for attendees to connect with colleagues as well as learn about the latest products in the design and verification industry. As of this writing, we have 20 exhibitors participating in the virtual exhibit hall.

My sincere thanks to our program sponsor, Accellera Systems Initiative, industry sponsors, steering committee volunteers, technical program committee volunteers, past chairs and Conference Catalyst staff who have worked hard to put together a program that makes DVCon "the" conference for design and verification engineers.

I sincerely look forward to "seeing" you online at DVCon U.S. 2021!

Aparna Dey
DVCon U.S. 2021 General Chair

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CONFERENCE SPONSOR

Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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John Dickol, Samsung

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Vanessa Cooper, Verilab, Inc.

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Tom Fitzpatrick, Siemens EDA

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CONFlux Platform

URL: dvcon-us-virtual.org

This platform will be used for the following:

- Display DVCon U.S. Schedule with live Zoom links to sessions
- Provide networking opportunities to connect with fellow attendees, exhibitor & sponsors through engagements, Discover DVCon, and the Best Paper Rating System.
- Exhibit spaces for all sponsors & exhibitors
- Live session recordings will be posted on the platform for viewing after the sessions take place
- There will be opportunities to ask questions on presentations synchronously and asynchronously so authors can respond throughout the conference
- The platform will be accessible to registrants through **March 31, 2021**

Engagement

Engagement is a feature within CONFLUX (DVCON U.S. 2021 Virtual Platform) that allows attendees, speaker, sponsor and exhibitors to connect in real time. This tool allows you to conference call or video call with up to 50 participants at any time. To access the feature, login into the virtual platform and click "Engagement" in the left column menu bar.

1. **Scheduled Engagements:**
   a. Sponsors and Exhibitors have been given the opportunity to schedule 1 or more engagement sessions depending on their sponsorship level for attendees to participate in. These sessions will be organized and lead by the sponsors and exhibitors. The sessions range from 30 minutes to an hour and can consist of networking, presentations, demonstrations, and more. All sessions will occur during Networking/Exhibit Hall hours.

1. **Hallway Engagements:**
   a. Hallway engagements are spontaneous sessions that can be started by any attendee, speaker, sponsor, or exhibitor. Invite any activeparticipant that is active on the platform to join a conference call or video call to continue discussions for technical session or to connect/network. These sessions will not be listed on the program or engagement schedule and will be by invitation only. Hallway engagements are available 24/7 from March 1st to March 4th.

Best Paper/Poster Rating System

Attendees registered under an ALL-ACCESS pass will be able to rate all paper and poster presentations they attend. At the conclusion of the live session visit the presentations profile to rate each individual presentation. The rating scale will be from one to five. The top presentations should receive a 5-star rating. Rating will open on March 2nd at 9:00 PST and close on March 3rd at 16:45 PST.

On March 3rd at 17:00 PST the Best Paper/Poster Presentation Award Ceremony will occur.

Each attendee can only rate a presentation once. The TPC will average the rating on each presentation to reach the final scores. The top 3 rated papers and the top 3 rated posters will be recognized during the Award Ceremony on March 3rd.

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Discover DVCon: Make the most of your virtual conference experience!

DVCON U.S. 2021 is pleased to offer Discover DVCon, an incentive program designed to help attendees experience all aspects of the virtual conference while also being entered to win a range of prizes.

The game is laid out to encourage each attendee to visit, interact, and network with as many sponsors, exhibitors and other attendees as possible. One important feature the virtual platform facilitates and encourages is engagements. Sponsors and exhibitors will have scheduled engagement periods scattered throughout the conference during Networking/Exhibit Hall hours. Participation in sponsor or exhibitor networking, presentation or demonstration opportunities will earn the attendee points. At the end of the conference, attendees with at least 20 points will be entered to when a prize.

How to play?

1. Discover DVCon will begin on March 1st at 16:00 PST and end at March 4th at 13:30 PST.
2. Be actively logged into the virtual platform during Networking/Exhibit Hall hours (see the program for specific times).
3. Click the icon "Sponsors" in the left column menu bar.
4. Familiarize yourself with the DVCON U.S. 2021 Sponsors & Exhibitors. The company's virtual space/booth will include overview details, videos, flyers, contact information and more. This information will help you plan out your week and enable you to get connected with representatives.
5. A button will be located on each virtual space/booth. Click this button to earn your points.
6. Next click the icon "Engagements" in the left column menu bar or link directly to the scheduled engagement from the sponsor or exhibitor's virtual space/booth.
7. At the scheduled engagement time, join the session by clicking the "Join Session" button.
8. In the top right corner of the video screen will be a button. Click this button to earn additional points.
9. The more virtual spaces, booths and engagements you participate in, the more points you will receive.

How points will be calculated?

1. You will receive 1 point for every virtual space/booth visited and 2 points for every scheduled engagement participated in.
2. Points can only be gained during Networking/Exhibit Hall hours.
3. The virtual platform will automatically track your points.

Prizes:

- Win gift cards with values ranging from $100 to $500 USD or complimentary registration to attend DVCon U.S. 2022.

We understand that these are unprecedented times but we hope that through CONFLUX and Discover DVCon we can help our attendees, sponsors and exhibitors make the most of their virtual experiences. DVCON U.S. 2021 has a variety of high-quality presentations from our authors, invited speakers and sponsored speakers. Attendees are encouraged to check out all aspects of the platform, live and on-demand, to maximize their conference experience.

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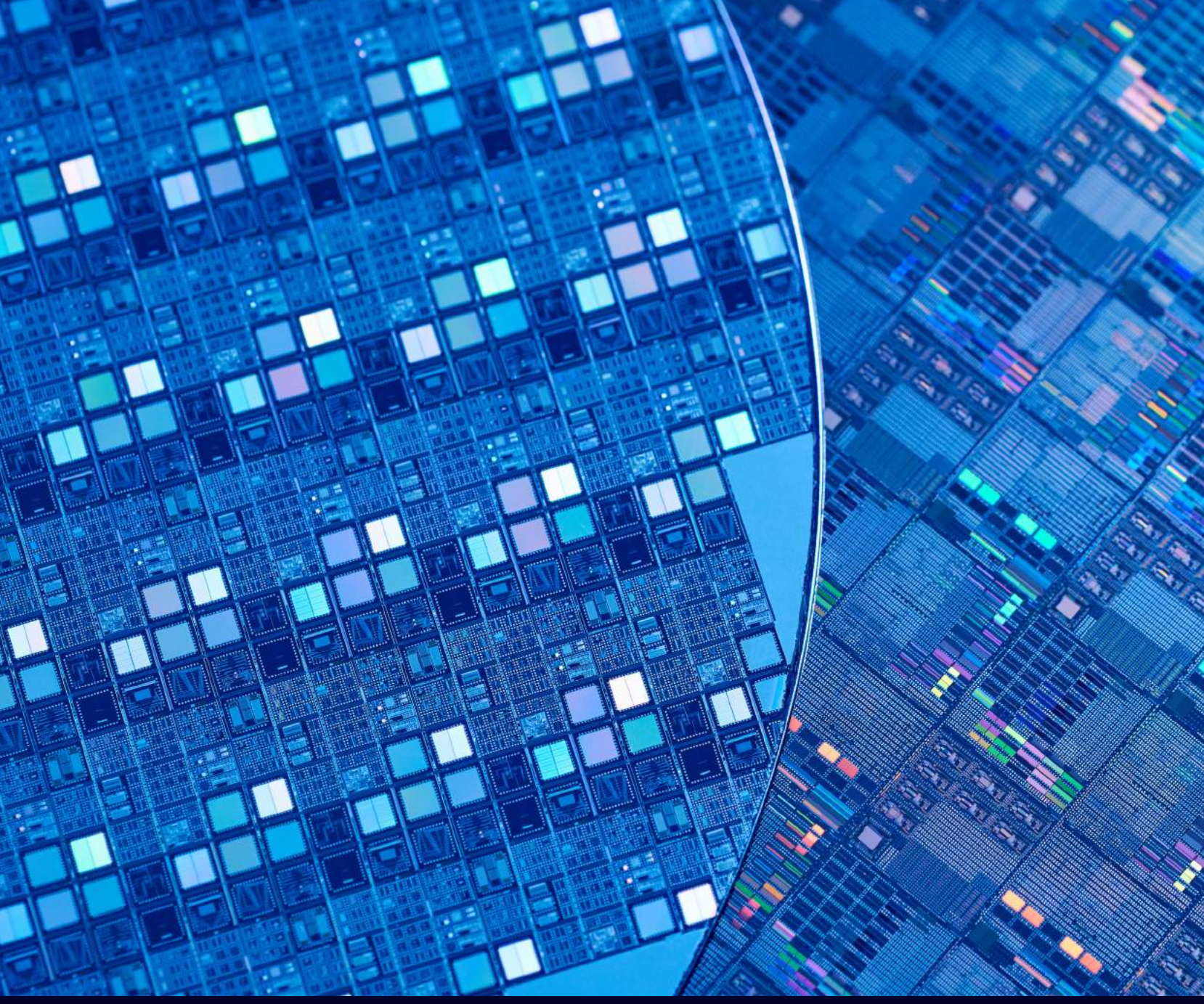
DVCon U.S. 2021 - Technical Program
March 1, 2021

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3	Zoom Room #4
9:00 - 10:00	**Tutorial:** Portable Stimulus 2.0 Is Here: What You Need to Know *(Presented by members of Accellera's Portable Stimulus Working Group)*	**Workshop:** UVM-SystemC Randomization - Updates from the SystemC Verification Working Group *(Presented by members of Accellera's SystemC Verification Working Group)*	**Workshop:** Getting to Know Accellera's Emerging Hardware Security Standard: Security Annotation for Electronic Design Integration *(Presented by members of Accellera's IP Security Assurance Working Group)*	**Workshop:** System-Level Power Analysis with IEEE 2416 Power Models *(IEEE)*
10:00 - 11:00				UVM Birds of a Feather
11:00 - 11:30	**Break**			
11:30 - 12:30	**Workshop:** UVM-AMS: A UVM-Based Analog Verification Standard *(Presented by members of Accellera's UVM-AMS Working Group)*	**Workshop:** Multi Language Verification Framework Standardization and Demo *(Presented by members of Accellera's Multi-Language Working Group)*	**Workshop:** An Introduction to the Accellera Functional Safety Working Group Standardization Effort *(Presented by members of Accellera's Functional Safety Working Group)*	
12:30 - 13:30	**Lunch Break**			
13:30 - 14:30	**Workshop:** Verification of Functional Safety for an Automotive Ai Processor *(Veriest Solutions)*	**Workshop:** Early Design and Validation of an Ai Accelerator's System Level Performance Using an HLS Design Methodology *(Siemens EDA)*	**Workshop:** Functional SoC and Early Firmware Verification Using a Virtual Realization Layer *(Breker Verification Systems)*	
14:30 - 15:00	**Break**			
15:00 - 16:00	**Workshop:** Harmonizing Hardware and Software – Inside the Engineer's Head *(Semifore)*	**Workshop:** Smarter Verification Management *(Cadence Design Systems)*	**Workshop:** Achieving ISO 26262 ASIL Metrics Using Modern Static and Dynamic Failure Mode Fault Analysis *(Optima Design Automation)*	
16:00 - 17:00	**Networking/Exhibit Hall Open**			



DVCon U.S. 2021 - Technical Program
March 2, 2021

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3	Zoom Room #4	Zoom Room #5	Zoom Room #6
8:00 - 8:30	Opening Session					
8:30 - 9:00	Break					
9:00 - 10:30	Debug Analysis 1	Portable Stimulus	Verification Languages			
10:30 - 12:00	Poster: CDC	Poster: HW/SW Co-Verification	Poster: Modeling and Patterns	Poster: Prototyping and Emulation	Poster: Verification Methodologies	Poster: Verification Processes
12:00 - 13:00	Lunch Break					
13:00 - 14:15	Keynote: Dr. Paul Cunningham					
14:00 - 17:00	Networking/Exhibit Hall Open					
15:00 - 17:00	Advanced Methodologies 1	Advanced Methodologies 2	UVM and RISC-V			

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DVCon U.S. 2021 - Technical Program
March 3, 2021

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3
8:30 - 9:30	**Panel:** Verification in the Open-Source Era		
9:30 - 10:00	**Break**		
10:00 - 12:00	**Automation using Machine Learning**	**Formal Verification**	**Mixed-Signal Design**
12:00 - 13:00	**Lunch Break**		
13:00 - 14:00	**Panel:** Chip Design on Cloud - from Pipe Dream to Preeminence?		
14:00 - 15:00	**Networking / Exhibit Hall Open**		
15:00 - 16:30	**Debug Analysis 2**	**Low Power Design and Verification**	**Verification Potpourri**
17:00 - 17:15	**Best Paper Presentation**		
17:00 - 18:00	**Networking/Exhibit Hall Open**		

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DVCon U.S. 2021 - Technical Program
March 4, 2021

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3
9:00 - 11:00	**Tutorial:** Raising the Verification Bar: Cloud based Simulation Increases Verification Efficiency *(Synopsys, Inc.)*	**Tutorial:** Applying Big Data to Next-Generation Coverage Analysis and Closure *(Siemens EDA)*	**Tutorial:** Benefits of a Common Methodology for Emulation and Prototyping *(Cadence Design Systems)*
11:00 - 11:30	**Break**		
11:30 - 12:30	**Workshop:** RISC-V Based SoC Design, Verification, and Validation in One Hour *(Agnisys, Inc.)*	**Workshop:** Functional debug: Verification and Beyond *(Siemens EDA)*	**Workshop:** Accelerate Signoff with JasperGold RTL Designer Apps *(Cadence Design Systems)*
12:30 - 13:30	**Networking / Exhibit Hall Open**		
13:30 - 14:30	**Workshop:** Beyond Bug Hunting: Verification Coverage from Safety to Certification *(OneSpin Solutions)*	**Workshop:** Shift Left: Cloud As the Technology Platform to Enable Faster Verification *(Google, LLC)*	**Workshop:** Fast Forward Your Product Launch Using Shift Left - Hardware-Software co-Design & co-Verification Using ESL Methodologies *(Circuitsutra Technologies Pvt Ltd)*

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Technical Program: Monday, March 1
Time Zone is PST

9:00 - 11:00
Tutorial: Portable Stimulus 2.0 Is Here: What You Need to Know
Presented by members of Accellera's Portable Stimulus Working Group

By: **Tom Fitzpatrick**, Siemens EDA; **Adnan Hamid**, Breker Verification Systems; **Matan Vax,** Cadence Design Systems; **Faris Khundakjie**, Intel; **Karthick Gururaj**, Vayavya Labs; **Hillel Miller**, Synopsys

The Portable Test and Stimulus Standard (PSS) from Accellera lets you create a single representation of stimulus and test scenarios that are usable by a variety of users across different platforms and different integration levels throughout a verification project. This tutorial will share some of the important new features coming in v2.0 that were added to enhance the usability, programmability and portability of PSS.

9:00-10:00
Workshop: UVM-SystemC Randomization - Updates from the SystemC Verification Working Group

Presented by members of Accellera's SystemC Verification Working Group

By: **Thilo Voertler**, COSEDA Technologies GmbH
Dragos Dospinescu, AMIQ

Contributions to the Workshop presentation are also provided by:
Martin Barnasconi, NXP Semiconductors
Stephan Gerth, Bosch Sensortec GmbH

This workshop will introduce the basic concepts of UVM-SystemC and show how constrained randomization and functional coverage can be integrated to build a verification environment using the current UVM-SystemC library. Currently, the Accellera VWG is working on the standardization of a common randomization layer based on CRAVE, a C++, and SystemC constraint randomization library. The workshop will show how constrained randomization can be used within SystemC and integrated into UVM-SystemC verification environments.

9:00-10:00
Workshop: Getting to Know Accellera's Emerging Hardware Security Standard: Security Annotation for Electronic Design Integration

Presented by members of Accellera's IP Security Assurance Working Group

By: **Jean-Philippe Martin**, Intel; **Brent Sherman**, Intel; **John Hallman**, Onespin

This session will introduce an emerging new standard called Security Annotation for Electronic Design Integration (SA-EDI) to address security concerns in a manner that is low-overhead, non-disruptive, and scalable across IP families. The standard specifies an approach to provide information about the IP security relevant to the integrator and recommended mitigations to implement and risk to address. At the conclusion of this session, attendees will better understand risks associated with IP and become familiar with the SA-EDI standard, including how it can be applied and when it will be available for reference.

9:00–10:00
Workshop: System-Level Power Analysis with IEEE 2416 Power Models
IEEE

By: **Jerry Frenkil**, Si2; **Nagu Dhanwada**, IBM; **Rhett Davis**, North Carolina State University; **David Ratchkov**, Thrace Systems

This workshop will describe the new power modeling standard, IEEE 2416, the novel tools and methodologies it enables, and the inter-operation of 2416 power data models with IEEE 1801 power state models. 2416 addresses the power modeling needs of three distinct groups of users: IP providers, System Architects and System Validation teams, and EDA developers. Use of 2416 by each group will be described using a memory model and a RISC-V processor model with an Energy per Instruction format.

10:30–11:30
UVM Birds of a Feather

By: **Tom Fitzpatrick**, Siemens EDA; **Mark Strickland**, **Marvell** and **Justin Refice**, NVIDIA; **Lakshamanan Balasubramanian**, Texas Instruments

The Accellera UVM Working Group has recently delivered a UVM library to match the IEEE 1800.2-2020 specification and is now considering which enhancements and bug fixes to work on next that would most benefit the user community. A complication is that many in the user community are still using older versions of UVM and so would not benefit from improvements to the 1800.2-2020 library. This session will gather feedback from the user community to understand what could be done to help users get to 1800.2-2020 as well as what types of improvements would be the most useful.

We will go through a brief history of UVM development in order to understand how we ended up with various versions that are not 100% compatible with each other. We will present the ideas that the Working Group are considering to expedite migration to the latest version and the ideas for future enhancements. Then we will use Zoom polling to get a feeling for the current status and the preferences of the audience. We will conclude with a live Q&A session to gather any feedback that could not be expressed through the polling.

11:00–11:30
Break

11:30–12:30
Workshop: UVM-AMS: A UVM-Based Analog Verification Standard

Presented by members of Accellera's UVM-AMS Working Group

By: **Patrick Lynch**, Xilinx; **Xiang Li**, Qualcomm; **Shekar Chetput**, Cadence; **Joen Westendorp**, NXP

Key members of the Accellera UVM-AMS Working Group will share the work done so far in developing a comprehensive and unified analog/mixed-signal verification methodology based on UVM to improve analog mixed signal (AMS) and digital mixed signal (DMS) verification of integrated circuits and systems.

11:30–12:30
Workshop: Multi Language Verification Framework Standardization and Demo

Presented by members of Accellera's Multi-Language Working Group

By: **Warren Stapleton**, AMD; **Bryan Sniderman**, AMD; **Alex Chudnovsky**, Cadence; **Faris Khundakjie**, Intel; **Martin Barnasconi**, NXP

In this Workshop, the MLVWG presents the current status of the proof-of-concept implementation and demonstrate its capabilities. A multi-language example is presented, which combines the Universal Verification Methodology (UVM) library in SystemVerilog and SystemC. Based on this example, the multi-language verification framework, its foundation concepts and the API targeted for standardization is explained and discussed. In addition, multi-language-specific UVM standardization requirements will be presented and language extensions are proposed to address seamless integration and interoperability between UVM verification frameworks in SystemVerilog and SystemC.

11:30–12:30
Workshop: An Introduction to the Accellera Functional Safety Working Group Standardization Effort

Presented by members of Accellera's Functional Safety Working Group

By: **Alessandra Nardi**, Cadence

Presenters: **Oscar Ballan**, Ethernovia; **TBD**, ST Microelectronics; **Ghani Kanawati**, ARM

Accellera formed a working group of functional safety practitioners and experts from the industry to develop a standard that will provide a standardization definition of the Functional Safety data exchange to improve automation, interoperability, and traceability of the implementation of the Functional Safety guidelines and best practices during the lifecycle. The standard plans to capture a data model, language, or format to exchange data seamlessly among functional safety work products and across layers of the supply chain. This workshop presents some of the challenges in the industry for managing the exchange of data related to functional safety and then the goals and mission of the Accellera Functional Safety Working Group towards a new standard to address those challenges.

12:30–13:30
Lunch Break

13:30–14:30
Workshop: Verification of Functional Safety for an Automotive Ai Processor
Veriest Solutions

By: **Mihajlo Katona**, Veriest Solutions

This presentation is addressing the handling of random failures during the design and verification of the CEVA IPs designed to be parts of a complex automotive system. By analyzing architectural aspects of modern integrated circuits we will identify critical design features and we will review principles for verification of safety mechanisms based on an example of an AI processor for on-chip deep learning inferencing, computer vision tasks, and fusing data from multiple sensors such as radar, lidar, time-of-flight, microphones, and other inertial measurement units.

13:30–14:30

Workshop: Early Design and Validation of an Ai Accelerator's System Level Performance Using an HLS Design Methodology

Siemens EDA

By: **Michael Fingeroff**, Siemens EDA

This workshop will show how an HLS design and verification flow built around Catapult, and the ecosystem around it, could dramatically speed up the design of the AI/ML hardware accelerators compared to a traditional RTL based flow. It will focus on using the open-source MatchLib SystemC library from NVIDIA to perform rapid modelling and synthesis of the ML accelerator. The workshop will demonstrate how pre-hls simulation using MatchLib can identify and fix potential system-level performance issues that are normally not found till very late in a hand-coded RTL design methodology. Finally we will present 2-3 customer case-studies showcasing how these technologies work in conjunction to address our customers HLS design and verification challenges.

13:30–14:30

Workshop: Functional SoC and Early Firmware Verification Using a Virtual Realization Layer

Breker Verification Systems

By: **Adnan Hamid**, Breker Verification Systems

SoC Verification has become more important in recent years. However, this task is challenging given the increased complexity of UVM for larger systems, emulation usage and the need to drive processors as part of the system. This tutorial will provide a methodology using a virtual realization layer, as suggested by the PSS committee, which can perform various OS-like capabilities while streamlining hardware verification tool usage. It may also be used to aid firmware verification with the hardware.

14:30–15:00

Break

15:00–16:00

Workshop: Harmonizing Hardware and Software – Inside the Engineer's Head

Semifore

By: **Josh Rensch**, Semifore; **Rich Weber**, Semifore; **Jamsheed Agahi**, Semifore

The tape out used to be the end of a chip design project. Now, it's just the beginning. The chip needs to work in the system. And that means hardware, software, firmware, third party IP and exotic packaging technology all need to work in harmony. Today's SoCs are highly complex endeavors involving many contributors from many different disciplines. And they all need to be coordinated.

In this Workshop, we'll explore the challenges of harmonizing hardware and software design for SoC projects. The format will be informal conversations with three experts in this field. Josh Rensch from Semifore will do the interviewing. He'll be talking with Dave Burgoon, Principal Design Verification Engineer at Microsoft Corporation, Richard Weber, Co-Founder and CEO at Semifore and Jamsheed Agahi, Co-Founder and VP Quality at Semifore.

During these interviews, the speakers will share their real-life perspectives regarding hardware/software design – what's important and what they learned. We'll also touch on standards. Where they work and where they fall short. Attendees with gain relevant, actionable information to help them with their next design project as well as have the opportunity to talk live with all panelists during a lively Q&A session after the interviews.

15:00–16:00
Workshop: Smarter Verification Management
Cadence Design Systems

By: **Matt Graham**, Engineering

This workshop will demonstrate methods for addressing throughput, analysis efficiency and traceability utilizing features provided in the latest, fourth generation, architecture of Cadence Manager Verification Management solution. Specific solutions addressed will include supporting geographically distributed verification teams, cloud based regression farms, auto failure classification, open verification data APIs, and robust connections to functional specifications and requirements management systems.

15:00–16:00
Workshop: Achieving ISO 26262 ASIL Metrics Using Modern Static and Dynamic Failure Mode Fault Analysis
Optima Design Automation

By: **Sesha Sai Kumar**, Optima Design Automation;
Jamil Mazzawi, Optima Design Automation

Automotive Functional Safety Analysis under the ISO 26262 standard has evolved over the last few years, as the challenges have become better understood and respective solutions refined. Early approaches to demonstrate that devices meet specific Automotive Safety Integrity Level (ASIL) requirements have given way to more effective techniques and technologies. In this workshop we present new solutions that accelerate and increase the accuracy of this development phase.

16:00–17:00
Networking/Exhibit Hall Open

imperas

Taking the RISK out of RISC-V

ISA Configurability
Optimized Custom Instructions

RISC-V Processor Verification

Functional coverage, debug and analysis tools
RISC-V Architectural validation test suites
Imperas RISC-V Golden Reference Model
SystemVerilog UVM Step-and-Compare
Imperas Verification IP for RISC-V

Visit the Imperas booth at DVCon 2021
https://www.imperas.com/riscv

Technical Program: Tuesday, March 2
Time Zone is PST

8:00–8:30
Opening Session

8:30–9:00
Break

9:00–10:30
Debug Analysis 1

Session Chair:
Kelly Larson, Tesla
Stephen Donofrio, Paradigm Works

DeltaCov: Automated Stimulus Quality Monitoring System
Nimish Girdhar, NVIDIA
Srinivas Badam, NVIDIA

How to Overcome Editor Envy: Why Can't My Editor Do That?
Dillan Mills, Microchip Technology Inc.
Chuck McClish, Microchip Technology Inc.

Novel Paradigm in Formally Verifying Complex Algorithms
M. Achutha Kirankumar V, Intel Corporation
Disha Puri, Intel Corporation
Mohit Choradia, Intel Corporation
Paras Gupta, Intel Corporation

9:00–10:30
Portable Stimulus

Session Chair
Tom Fitzpatrick, Siemens EDA
Phu Huynh, Cadence Design Systems

Adopting Accellera's Portable Stimulus Standard: Early Development and Validation Using Virtual Prototyping
Simranjit Singh, Samsung Semiconductor India R&D Center
Ashwani Aggarwal, Samsung Semiconductor India R&D Center
Harshita Prabha, Samsung Semiconductor India R&D Center
Vishnu Ramadas, Samsung Semiconductor India R&D Center
Seonil Brian Choi, Samsung Electronics Co., Ltd.
Woojoo Space Kim, Samsung Electronics Co., Ltd.

Acceleration of Coreless SoC Design-Verification Using PSS on Configurable Testbench in Multi-Link PCIe Subsystems
Thanu Ganapathy, Samsung Semiconductor India R&D Center
Pravin Kumar, Samsung Electronics Co., Ltd.
Garima Srivastava, Samsung Semiconductor India R&D Center
Seonil Brian Choi, Samsung Electronics Co., Ltd.
Harish Peta, Cadence Design Systems

Media Performance Validation in Emulation and Post Silicon Using Portable Stimulus Standard
Suresh Vasu, Intel Corporation
Nithin Venkatesh, Intel Corporation
Joydeep Maitra, Intel Corporation

Technical Program: Tuesday, March 2 (cont.)
Time Zone is PST

9:00–10:30
Verification Languages

Session Chair:
Srivatsa Vasudevan, Cortina
Don Mills, Microchip

Configuration Conundrum: Managing Test Configuration With a Bite Sized Solution
Kevin Vasconcellos, Verilab, Inc.
Jeff McNeal, Verilab, Inc.

Lay It on Me: Creating Layered Constraints
Bryan Morris, Ciena Corp
Andrei Tarnauceanu, BTA Design Services

Verification Learns a New Language: – An IEEE 1800.2 Implementation
Ray Salemi, Siemens EDA
Tom Fitzpatrick, Siemens EDA

10:30–12:00
Poster: CDC

Session Chair:
Kamel Belhous, Teradyne
Kaiming Ho, Independent

Preventing Glitch Nightmares on CDC Paths: the Three Witches
Jian-Hua Yan, MediaTek Inc.
Ping Yeung, Siemens EDA
Stewart Li, Siemens EDA
Sulabh-Kumar Khare, Siemens EDA

Reset Domain Crossing for Designs With Set-Reset Flops
Abdul Moyeen, Siemens EDA
Inayat Ali, NXP Semiconductors

Strategies on CDC False Alarm Rapid Location
Jian-Hua Yan, MediaTek Inc.
Meiling Qi, MediaTek Inc.
Yunyang Song, MediaTek Inc.

Evolution of CDC Recipe: Learning Through Real Case Studies and Methodology Improvements
Amit Kulkarni, Intel Corporation
Suhas DS, Intel Corporation
Deepmala Sachan, Intel Corporation

10:30–12:00
Poster: Verification Methodologies

Session Chair:
Erik Seligman, Intel Corp.

"Bounded Proof" Sign-Off With Formal Coverage
Abhishek Anand, Intel Corporation
Chinyu Chen, Intel Corporation
Bathri Subramanian, Siemens EDA
Joe Hupcey, Siemens EDA

A Semi-Formal Verification Methodology for Efficient Configuration Coverage of Highly Configurable Digital Designs
Aman Kumar, Chipglobe GmbH
Sebastian Simon, Infineon Technologies / Dresden GmbH & Co. KG

10:30–12:00
Poster: Verification Processes

Session Chair:
Neel Sonara, Broadcom
Christine Thomson, Microsoft

Strategies and Methods of using PSS2.0 high level modeling techniques to augment UVM verification
Swami Venkatesan, Cadence Design Systems

Automated Traceability of Requirements in the Design and Verification Process of Safety-Critical Mixed-Signal Systems
Gabriel Pachiana, Fraunhofer IIS/EAS
Maximilian Grundwald, Fraunhofer IIS/EAS
Thomas Markwirth, Fraunhofer IIS/EAS
Christoph Sohrmann, Fraunhofer IIS/EAS

Accelerating SoC Verification Signoff Using Save & Restart/Dynamic Test Reload Enhanced Regression Flow
Vanshlata Baby, Samsung Semiconductor India R&D Center
Divya Madhavrapu, Samsung Semiconductor India R&D Center
Garima Srivastava, Samsung Semiconductor India R&D Center
Seonil Brian Choi, Samsung Electronics Co., Ltd

12:00–13:00
Lunch Break

10:30–12:00
Poster: HW/SW Co-Verification

Session Chair:
Progyna Khondkar, Siemens EDA

Abstract Layer for Firmware Access: A Unique Approach for SOC Functional Verification
Girish Kumar Gupta, Samsung Semiconductor India R&D Center
Navia Vishnu Rugmini, Samsung Semiconductor India R&D Center
Praval Choudhary, Samsung Semiconductor India R&D Center
Mobeenuddin Syed, Samsung Semiconductor India R&D Center

Generic SCSI-Based Host Controller Verification Framework Using System Verilog
Mohamed Rayan, Siemens EDA
Mohamed Samy, Siemens EDA
Haytham Ashour, Siemens EDA
Ashraf Salem, Siemens EDA

10:30–12:00
Poster: Modeling and Patterns

Session Chair:
Srivatsa Vasudevan, Cortina
Progyna Khondkar, Siemens EDA

An Equivalent Modeling Approach for High-Density DRAM Array System-Level Design-Space Exploration in System Verilog
Seyoung Kim, Seoul National University/Samsung Electronics
Jaeha Kim, Seoul National University

10:30–12:00
Poster: Prototyping and Emulation

Session Chair:
John Dickol, Samsung

Conversion of Performance Model to Functional Model|
H G Pavan Kumar, Samsung Semiconductor India R&D Center
Sumail Singh Brar, Samsung Semiconductor India R&D Center
Ashwani Aggarwal, Samsung Semiconductor India R&D Center
Seonil Brian Choi, Samsung Electronics Co., Ltd.
Woojoo Space Kim, Samsung Electronics Co., Ltd.

Improving Software Testing Speed by 100X With SystemC Virtualization in IoT Devices
David Barahona, Norwegian University of Science and Technology
Motaz Thiab, Norwegian University of Science and Technology
Isael Díaz, Nordic Semiconductor
Joakim Urdahl, Nordic Semiconductor
Milica Orlandic, Norwegian University of Science and Technology

13:00-14:15

Keynote Presentation:
Computational Logistics for System and Software Verification

By: **Dr. Paul Cunningham**

Bio: Paul Cunningham is corporate vice president and general manager of the system verification group at Cadence. His product responsibilities include logic simulation, emulation, prototyping, formal verification, Verification IP, and debug. Prior to this, he was responsible for Cadence's frontend digital design tools including logic synthesis and design-for-test. Paul joined Cadence in 2011 through the acquisition of Azuro, a startup developing concurrent physical optimization and useful skew clock tree synthesis technologies, where he was a co-founder and CEO.

Paul holds a Master's Degree and a Ph.D. in Computer Science from the University of Cambridge in the UK.

Abstract: Modern SoC designs are complex multi-billion gate compute systems containing multi-core CPUs, GPUs, DSPs, multimedia accelerators, and AI accelerators. Verification of these devices and their software stacks requires a new throughput-centric mindset that considers the cost of tools, compute, and people, as well as the relative abilities of each, to accelerate verification. In this talk, Dr. Cunningham will introduce the concept of verification throughput and highlight the significant opportunities we have as an industry to dramatically improve verification throughput on modern SoC designs.

14:00-17:00

Networking/Exhibit Hall Open

15:00-17:00

Advanced Methodologies 1

Session Chair:

Kaiming Ho, Independent
Dave Rich, Siemens EDA

An Efficient Method to Verify Dynamic IP Clock Frequency on SOC Level by Using Auto-Generated Active Clock Monitor

Jaecheon Kim, Samsung Electronics Co., Ltd.
Gyuhong Lee, Samsung Electronics Co., Ltd.
Yeonho Jeong, Samsung Electronics Co., Ltd.
Hyunsun Ahn, Samsung Electronics Co., Ltd.
Daewoo Kim, Samsung Electronics Co., Ltd.
Seonil Brian Choi, Samsung Electronics Co., Ltd.

Synthesizable Random Testbench for Multimedia IP Verification

Sanggyu Park, Samsung Electronics Co., Ltd.

Hardware Trojan Design and Detection With Formal Verification to Deep Neural Network

Si-Han Chen, National Cheng Kung University
Yu-Ting Huang, National Cheng Kung University
Yi-Chun Kao, National Cheng Kung University
Yean-Ru Chen, National Cheng Kung University
Shang-Wei Lin, Nanyang Technological University
Chia-I Chen, Realtek Semiconductor Corp

Making Your DPI-C Interface a Fast River of Data

Rich Edelman, Siemens EDA

15:00-17:00
Advanced Methodologies 2

Session Chair:
Paul Marriott, Verilab
Ning Guo, AMD

Detecting Circular Dependencies in Forward Progress Checkers
Saurabh Chaurdia, Oski Technology
Arun Khurana, Oski Technology
Naveen Kumar, Oski Technology
Aditya Chaurasiya, Oski Technology
Yogesh Mahajan, NVIDIA
Prasenjit Biswas, NVIDIA

An Automated Validation Framework for Power Management and Data Retention Logic Kits of Standard Cell Library
Akshay Kamath, Samsung Semiconductor India R&D Center
Bharath Kumar, Samsung Semiconductor India R&D Center
Sunil Aggarwal, Samsung Semiconductor India R&D Center
Subramanian Parameswaran, Samsung Semiconductor India R&D Center
Parag Lonkar, Samsung Semiconductor India R&D Center
Debi Prasanna, Samsung Semiconductor India R&D Center
Somasunder Kattepura Sreenath, Samsung Semiconductor India R&D Center

Methodology for Automating Coverage-Driven Interrupt Testing of Instruction Sets
David McConnell, EM Microelectronic-US, Inc.
Greg Tumbush, EM Microelectronic-US, Inc

Addressing Challenges in Verification of DSP Based Audio IPs Using a Novel Hybrid-Testbench Architecture
Suvadeep Bose, Samsung Semiconductor India R&D Center
Kanak Rajput, Samsung Semiconductor India R&D Center
Parag Lonkar, Samsung Semiconductor India R&D Center
Somasunder Kattepura Sreenath, Samsung Semiconductor India R&D Center

15:00-17:00
UVM and RISC-V

Session Chair:
Vibarajan Viswanathan, Samsung
Logie Ramachandran, Accelver Systems Inc.

RISC-V Processor Verification: Case Study
Adi Maymon, NVIDIA
Shay Harari, NVIDIA
Lee Moore, Imperas Software Ltd
Larry Lapides, Imperas Software Ltd

Jump Start Your RISCV Project With Open HW
Mike Thompson, OpenHW Group
Jingliang Wang, Futurewei Technologies, Inc
Steve Richmond, Silicon Labs
Lee Moore, Imperas Software Ltd
David McConnell, EM Microelectronic-US, Inc.
Greg Tumbush, EM Microelectronic-US, Inc.

Watch Out: Generating Coordinated Random Traffic in UVM
Nigasan Ragunathan, Microsoft Corporation
Christine Thomson, Microsoft Corporation

To Infinity and Beyond - Streaming Data Sequences in UVM
Mark Litterick, Verilab, Inc.
Jeff Vance, Verilab, Inc.
Jeff Montesano, Verilab, Inc.

Technical Program: Wednesday, March 3
Time Zone is PST

8:30–9:30
Panel: Verification in the Open-Source Era

Organizer:

Nanette Collins
Nanette V. Collins
Marketing & PR

Moderator:

Brian Bailey
Technology Editor/EDA
Semiconductor
Engineering

Panelists:

Bipul Talukdar/SmartDV
Simon Davidmann/
Imperas
Serge Leef/DARPA
Jean-Marie Brunet/
Siemens EDA
Ashish Darbari/Axiomise
Tao Liu/Google

The idea of open source hardware, such as RISC-V that anyone can leverage to create their own CPU or custom accelerator, is tantalizing. Supporters believe freely available solutions will break open processor innovation and enable entry into new market segments. Blocks of open source IP already are implemented or in the process of being implemented in many of today's chip designs. Success seems assured.

Verification groups are hopeful but leery knowing verification is a much more complex problem than design. Most open source hardware is new and does not have the benefit of field-proven experience, which means verification groups are on the line to devise an untried verification flow, making a well-considered CPU verification strategy fundamental. Without those ingredients, it is impossible to have confidence in verification results.

Semiconductor Engineering's Brian Bailey will take a panel of design verification experts and open source proponents on an excursion into the open-source era to analyze the verification challenges. His questions, meant to create debate and discussion, will include:

- Is open source verification more or less complex than design?
- Does open source verification mean that an engineer creates a SystemVerilog testbench and makes it freely available?
- Should the industry have a freely available open source reference model?
- The formal model for the RISC-V processor is written in SAIL, a language not traditionally supported by the EDA community. Will this lead to a departure in tool development?
- Some believe that for true open source, open source tools need to be available. Who will supply the funding for this development when major players already pay for the necessary tools?
- Can open source tools compete with tools that have seen long-term investment?
- What does compliance mean and how will it be enforced? Does compliance require open source verification environments? If so, what they would look like?
- Most processors are verified with a combination of formal and simulation methods? How will formal play in an open source world?

By the panel's conclusion, panelists will have attempted to answer why verification is essential for success of the open source movement.

Question for positioning statement: What does open source verification mean?

9:30–10:00
Break

10:00-12:00
Automation Using Machine Learning

Session Chair:
Dave Rich, Siemens EDA
Mark Azadpour, First Pass Eng.

Novelty-Driven Verification: Using Machine Learning to Identify Novel Stimuli and Close Coverage
Tim Blackmore, Infineon Technologies
Rhys Hodson, Infineon Technologies
Sebastian Schaal, Luminovo GmbH

Dynamically Optimized Test Generation Using Machine Learning
Rajarshi Roy, NVIDIA
Mukhdeep Benipal, NVIDIA
Saad Godil, NVIDIA

ML-Based Verification and Regression Automation
Abhishek Chauhan, Agnisys
Asif Ahmad, Agnisys;

Supporting Root Cause Analysis of Inaccurate Bug Prediction Based on Machine Learning – Lessons Learned When Interweaving Training Data and Source Code
Oscar Werneman, Verifyter
Markus Borg, RISE Research Institutes of Sweden
Daniel Hansson, Verifyter

10:00-12:00
Formal Verification

Session Chair:
Xiaolin Chen, Synopsys
Mitchell Poplingher, Lockheed Martin Corp.

Accelerating the IP Design Cycle With Formal Techniques Beyond Everyday FPV
Bhushan Parikh, Intel Corporation
Shaman Narayana, Intel Corporation
Buck Lem, Intel Corporation
David Cassetti, Intel Corporation

Metrics Driven Sign-Off for SoC Specific Logic (SSL) Using Formal Techniques
Abhinav Gaur, NXP Semiconductors
Gaurav Jain, NXP Semiconductors
Ruchi Singh, NXP Semiconductors

Can Formal Outsmart Synthesis: Improving Synthesis Quality of Results Through Formal Methods
Eldon Nelson, Synopsys

A Novel Approach to Verify CNN Based Image Processing Unit
Sumit Kumar Kulshreshtha, Intel Corporation
Raghavendra J N, Intel Corporation

Technical Program: Wednesday, March 3 (cont.)
Time Zone is PST

10:00–12:00
Mixed-Signal Design and Verification

Session Chair:
Neel Sonara, Broadcom
Kamran Haqqani, Maxim Integrated

A Volterra-Series Model in SystemVerilog/XMODEL for Nonlinear RF Low-Noise Amplifiers
Chan Young Park, Seoul National University
Jaeha Kim, Seoul National University

A Novel Variation-Aware Mixed-Signal Verification Methodology to Achieve High-Sigma Variation Coverage at Nanometer Designs
Tibi Galambos, Analog Value
Sumit Vishwakarma, Siemens EDA

Robust Physical Layer IP Verification for DDR4-3DS Memory by Channel Modelling
Aditya S Kumar, Samsung Semiconductor India R&D Center
Gowdra Bomman Chethan, Samsung Semiconductor India R&D Center
Shivani Maurya, Samsung Semiconductor India R&D Center
Kumar Rajeev Ranjan, Samsung Semiconductor India R&D Center
Anil Deshpande, Samsung Semiconductor India R&D Center
Somasunder Kattepura Sreenath, Samsung Semiconductor India R&D Center

Bi-Directional UVM Agents and Complex Stimulus Generation for UDN and UPF Pins
Chuck McClish, Microchip Technology Inc.

12:00–13:00
Lunch Break

13:00–14:00
Panel: Chip Design on Cloud -from Pipe Dream to Preeminence?

Panelists:
Ann Mutschler, Semiconductor Engineering
Megan Wachs, SiFive; Bob Lefferts, Synopsys
Eric Chesters, AMD
Richard Ho, Google LLC
Sashi Obilisetty, Google LLC

Gartner predicts that by 2025, about 80% of the datacenters will move to the cloud. Inherent benefits of the cloud, such as elasticity, fault tolerance, and security cannot be matched by on premise data centers. Indeed, cloud is the datacenter of choice for several industries from retail to banking to manufacturing.Chip design and verification on cloud has been a topic for decades (many among us remember the efforts of EDA companies in the early 2000s). However, the cloud - as it is today - is stunningly different. But what is the state of chip design on cloud? Are companies designing successfully on the cloud? Are migration efforts underway at companies? What works? What doesn't? Hear from a panel of designers and infrastructure experts on their experience with cloud. Learn about what works, what doesn't work or what cannot work!

14:00–15:00
Networking/Exhibit Hall Open

Technical Program: Wednesday, March 3 (cont.)
Time Zone is PST

15:00-16:30
Debug Analysis 2

Session Chair:
Kamel Belhous, Teradyne
Nagi Naganathan, Northrop Grumman

The Life of a System Verilog Variable
Dave Rich, Siemens EDA

Formal Verification Experiences: Spiral Refinement Methodology for Silicon Bug Hunt
Ping Yeung, Siemens EDA
Mark Eslinger, Siemens EDA
Jin Hou, Siemens EDA

Mechanism to Generate FIFO VC Dependency Graph and its Application to System Level Deadlock Verification
Debarshi Chatterjee, NVIDIA
Chad Parsons, NVIDIA
Siddhanth Dhodhi, NVIDIA

15:00-16:30
Low Power Design and Verification

Session Chair:
Amit Srivastava, Synopsys
Progyna Khondkar, Siemens EDA

Recipe for Bug Hunting: Tips & Tricks for Low Power Silicon Sign-Off
Monika Rawat, Intel Corporation
Dipankar Narendra Arya, Intel Corporation
Anuroop R, Intel Corporation
Deepmala Sachan, Intel Corporation

Primary, Anonymous, or What? The Destiny of Ports From Design Top That Ultimately Are Driven From Off-Chip…

Brandon Skaggs, Cypress Semiconductor
Progyna Khondkar, Siemens EDA

Melioration of Enhanced Low Power Memory Retention and Low Power Feature Validation Using API's

Nithin Venkatesh, Intel Corporation
Hareesh Akula, Intel Corporation

Technical Program: Wednesday, March 3 (cont.)

Time Zone is PST

15:00-16:30

Verification Potpourri

Session Chair:

Josh Rensch, Semifore

Bringing Reset Domains and Power Domains Together – Confronting Issues Due to UPF Instrumentation

Inayat Ali, NXP Semiconductors
Abdul Moyeen, Siemens EDA
Manish Bhati, Siemens EDA
Manjunatha Srinivas, Siemens EDA

Open-Source Framework for Co-Emulation Using PYNQ

Ioana Cătălina Cristea, Amiq Consulting
Dragos Dospinescu, Amiq Consulting

Advanced UVM, Multi-Interface, Reactive Stimulus Techniques

Clifford Cummings, Paradigm Works
Stephen Donofrio, Paradigm Works
Jeff Wilcox, Paradigm Works
Heath Chambers, HMC Design Verification

17:00-17:15

Best Paper Presentation

17:00-18:00

Networking/Exhibit Hall Open

Technical Program: Thursday, March 4
Time Zone is PST

9:00–11:00
Tutorial: Raising the Verification Bar: Cloud based Simulation Increases Verification Efficiency
Synopsys, Inc.

By: **Melvin Cardozo**, Synopsys
Ahmed Elzeftawi, Amazon

In this tutorial, architects from AWS, verification experts from Synopsys, and customers running simulation on the cloud will discuss these challenges and demonstrate a software development kit (SDK) including all the scripts required to setup a complete verification environment on the AWS. A joint solution between AWS and Synopsys has been developed to help customers bring their verification environments to AWS. This hands-on tutorial will include all the components essential to develop, compile, run and debug simulations in a cloud environment optimized for verification workloads. We will demonstrate how customers can easily deploy the Synopsys Verification Continuum® platform on AWS, making it easy to select the compute architecture of their choice, such as AMD EPYC, Arm-based AWS Graviton2, or Intel Xeon processors.

9:00–11:00
Tutorial: Applying Big Data to Next-Generation Coverage Analysis and Closure
Siemens EDA

By: **Tom Fitzpatrick**, Siemens EDA

Coverage closure remains the biggest functional verification challenge in our industry. This two-hour technical presentation will establish the need for a next-generation collaborative verification platform, providing enterprise-wide team-based shared coverage analytics and collaborative verification process integration, including lifecycle management integration. We will explore new ways of visualizing coverage data from different verification platforms – including simulation, emulation, FPGA and virtual prototyping and formal verification – to facilitate analytical navigation, and applying advanced analytics, including data mining and machine learning, to help your team identify functional coverage holes and effectively mobilize your verification team to reach coverage closure like never before.

9:00–11:00
Tutorial: Benefits of a Common Methodology for Emulation and Prototyping
Cadence Design Systems

By: **Michael Young**, product management;
Juergen Jaeger, product management

In this workshop, learn why you should consider bridging emulation and prototyping into a continuous verification environment to speed up your verification throughput for early software validation and real world testing. This workshop will cover:

- Fast design bring up between platforms (e.g. common implementation flow, common look & feel UI)
- Advanced debug (e.g. FullVision engine, probes, memory force and release, etc.)
- Re-usable system-level interfaces (real-world testing)

11:00–11:30
Break

Technical Program: Thursday, March 4 (cont.)
Time Zone is PST

11:30–12:30
Workshop: RISC-V Based SoC Design, Verification, and Validation in One Hour
Agnisys, Inc.

By: **Anupam Bakshi**, Agnisys, Inc.;
Abhishek Bora, Agnisys, Inc.

RISC-V brings a new wave to SoC development. Creating a fully validated design is an arduous process that takes several teams working together. Often the flow is a waterfall model where the specification is transformed in various stages of development. Sometimes aspects such as verification and validation are an afterthought. In order to speed up the process and get better quality of results, all aspects must be considered upfront.

11:30–12:30
Workshop: Functional debug: Verification and Beyond
Siemens EDA

By: **Hanan Moller**, Siemens EDA

In this workshop, we will explore an alternative approach to SoC development, analysis, debug and bring up. We will describe a different approach, in which debug and performance tuning is considered from the outset, by including within the SoC a light but independent infrastructure dedicated to bringing debug visibility across the entire SoC – an approach which is independent of CPU architecture. We will outline a methodology which includes local intelligence inside the SoC to select and communicate off-chip only those monitoring data which are significant and meaningful. In this workshop, we will further discuss the features of functional debug solutions and the benefits they bring throughout the SoC development process.

11:30–12:30
Workshop: Accelerate Signoff with JasperGold RTL Designer Apps
Cadence Design Systems

By: **Pete Hardee**, Marketing;
Kanwarpal Singh, Solutions Architect

In this workshop, we will take the attendees through using the JasperGold Superlint and CDC applications, which add formal verification technology and functional checks to these structural checks. The JasperGold technology supports the designers to identify the real problem violations, confirming fixes, and providing justification for waiving the violations that are not problematic. Additional automatic formal checks are provided for functional verification of many aspects of the design, using properties derived automatically from the RTL. Workshop attendees will learn how these JasperGold RTL Designer apps combine to "shift left" these checks, providing a much more complete level of automated verification. The result is that RTL designers are able to sign off higher quality, more robust and CDC/RDC-clean designs, months earlier in the project schedule.

12:30–13:30
Networking/Exhibit Hall Open

13:30–14:30 PST

Workshop: Beyond Bug Hunting: Verification Coverage from Safety to Certification
OneSpin Solutions

By: **Nicolae Tusinschi**, OneSpin Solutions

This workshop will explore how mutation analysis can have a positive impact on the safety of your design and provide the signoff confidence needed to achieve proper safety certification. In addition, the workshop will show how to achieve a meaningful integration of formal and simulation coverage metrics. A long-standing wish of many verification engineers and managers, coverage integration reduces effort overlap between simulation and formal and enables faster, more rigorous signoff.

13:30–14:30 PST

Workshop: Shift Left: Cloud As the Technology Platform to Enable Faster Verification
Google, LLC

By: **Rajiv Malhotra**, AMD
Peeyush Tungnawat, Google, LLC
Sashi Obilisetty, Google, LLC

Silicon design is getting more complex, but time-to-market schedules are shrinking. Design teams have to do more with the same number of engineers. Companies engaged in designing chips are finding it challenging to absorb the increasing complexity while meeting schedule demands. Inherent benefits of the cloud, such as elasticity, fault tolerance, and security can be successfully leveraged by design teams.At this workshop you will learn basics of getting your EDA workloads running on Google Cloud Platform, and understand some real world use cases.

13:30–14:30 PST

Workshop: Fast Forward Your Product Launch Using Shift Left - Hardware-Software co-Design & co-Verification Using ESL Methodologies
Circuitsutra Technologies Pvt Ltd

By: **Umesh Sisodia**, Circuitsutra Technologies Pvt Ltd
Swaminathan Ramachandran, Circuitsutra Technologies Pvt Ltd

The term 'Electronics System Level (ESL)' have been used in the industry for nearly two decades now. Different people use it in different context, with different meanings. It can be primarily generalized as the collection of methodologies that enables 'Hardware-Software Co-Design' and 'Raising the abstraction of chip design above RTL'. ESL methodologies are not supposed to replace the traditional RTL-GDS flow, but rather co-exist with existing flow and augment it to perform various advanced activities which are not feasible with traditional flow. It enables Pre-Silicon firmware development, Architecture exploration to optimize power & performance early in the cycle at system level, High-Level Synthesis (HLS), SoC Level simulation, System level simulation, Hardware-Software co-design and co-verification. In this workshop we will briefly touch upon various use cases of ESL methodologies and discuss the best practices being used in the industry.

Save the Date!
DVCon U.S. 2022
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